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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,997	08/07/2001	Hiroyuki Takahashi	SIM-01501	1911

26339 7590 02/11/2003

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EXAMINER	
COX, CASSANDRA F	
ART UNIT	**PAPER NUMBER**
2816	9

DATE MAILED: 02/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/923,997	Applicant(s) TAKAHASHI, HIROYUKI	
	Examiner Cassandra Cox	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *1-14 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

The indicated allowability of claims 7-8 and 13-14 is withdrawn in view of the new grounds of rejection.

1. Applicant's arguments with respect to claims 1-5, 9-11, and 15-18 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the high threshold p-MOS transistor that is connected to ground (in Figures 9 and 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because in Figure 9 the lines connecting the gates of the p-MOS transistors of inverters V92 and V94 and the n-MOS transistor of inverter V93 to their respective inputs are incomplete. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 9-11, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,970,694).

In reference to claim 1, Tanaka discloses in Figure 7 a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain (34-36) containing not less than one inverter; and a metal-oxide-semiconductor capacitor (40-42), known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter (34-36) and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein each stage is tied alternately to one of a power voltage source (VDD) and a ground voltage source (VSS). Tanaka does not disclose that the MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Applicant discloses in his specification that it is well known that p-MOS (or n-MOS) transistors having their gate connected to the output section of the inverter and their source and drains tied to a source voltage can be replaced with n-MOS (or p-MOS) transistors having their source and drains tied to the output section of the inverter and their gates tied to a source voltage. The two layouts

are equivalent to each other. Therefore it would have been obvious to one skilled in the art at the time of invention that you could use either layout (as called for in the claim) dependent on the desired outcome and the particular environment. The same applies to claims 2, 8, 14, 16 and 18.

In reference to claim 3, because the claimed structure is fully met by Tanaka, the recited function or "result" limitation "wherein a ratio of a gate voltage range of an on-state MOS capacitor to a gate voltage range of an off-state MOS capacitor is proportional to an increment or a decrement of the source voltage during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Tanaka, as held by the court in In re Best, 195 USPQ 430. The same applies to claim 9.

6. In reference to claim 4, because the claimed structure is fully met by Tanaka, the recited function or "result" limitation "wherein a value of the MOS capacitor changes in a direction to increase its capacitance during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Tanaka, as held by the court in In re Best, 195 USPQ 430. The same applies to claims 10 and 17.

7. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,970,694) in view of Hattori (U.S. Patent No. 5,459,424).

In reference to claim 5, Tanaka discloses all of the limitations as mentioned above with reference to claim 1, except that Tanaka does not disclose that the MOS capacitor (40-42) is represented by an n-MOS transistor. Hattori discloses in Figure 1 that the MOS capacitor is disposed on a transmission path of a logic signal, and is

represented by an n-MOS transistor (28) whose gate is connected to a node that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential (GND). It would have been obvious to one of skill in the art at the time of the invention that the MOS capacitors (28) of Hattori could be used in place of the MOS capacitor (40-42) of Tanaka as an example of one way of implementing a MOS capacitor. Since Tanaka does not disclose the type (n-type or p-type) of the MOS capacitors (40-42) used in the circuit any type could be used dependent on the particular type of environment. The same applies to claim 11.

8. Claims 6-7 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,970,694) in view of Porter et al. (U.S. Patent No. 6,040,713).

In reference to claim 6, Tanaka discloses all the limitations of the claim as mentioned above with reference to claim 1 except that Tanaka does not disclose that the MOS capacitor is represented by a p-MOS transistor. Porter discloses in column 6, lines 39-45 that the MOS capacitor (92, 94, 96, 98, 100) could also be represented by a p-MOS transistor whose gate is connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a ground potential. It would have been obvious to one of skill in the art at the time of the invention that the MOS capacitors (92, 94, 96, 98, 100) of Porter could be used in place of the MOS capacitor (40-42) of Tanaka as an example of one way of implementing a MOS capacitor. Since Tanaka does not disclose the type (n-type or p-type) of the MOS

capacitors (40-42) used in the circuit any type could be used dependent on the particular type of environment. The same applies to claim 12.

In reference to claim 7, Tanaka in view of Porter discloses all the limitation of the claim as mentioned above with reference to claim 6, except Tanaka does not disclose that the MOS capacitor is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage. Applicant discloses in his specification that it is well known that p-MOS (or n-MOS) transistors having their gate connected to the output section of the inverter and their source and drains tied to a source voltage can be replaced with n-MOS (or p-MOS) transistors having their source and drains tied to the output section of the inverter and their gates tied to a source voltage. The two layouts are equivalent to each other. Therefore it would have been obvious to one skilled in the art at the time of invention that you could use either layout (as called for in the claim) dependent on the desired outcome and the particular environment. The same applies to claim 13.

Allowable Subject Matter

9. Claim 15 is allowed.

10. The following is an examiner's statement of reasons for allowance: Claim 15 is allowed because the closest prior art of record fails to disclose a circuit as disclosed in the specification page 31, line 15 through page 32, line 1 wherein the low threshold voltage n-MOS transistors of each of a first and a third inverter are connected to ground

by a high threshold voltage n-MOS transistor; and low threshold voltage p-MOS transistors of each of a second and a fourth inverter are connected to ground by a high threshold p-MOS transistor; and said high threshold voltage n-MOS transistor and p-MOS transistor are set to an off state in response to a chip select signal and a chip select signal that is negated (respectively) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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February 9, 2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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